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Cascading Wafer-Scale Integrated Graphene Complementary Inverters under Ambient Conditions

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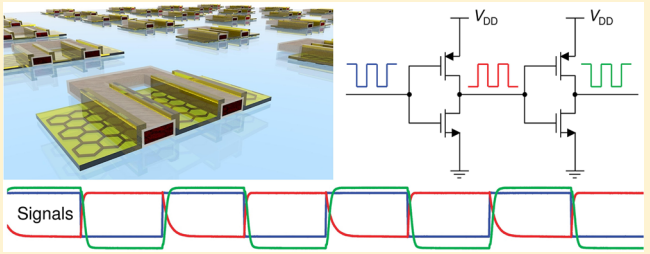
Supporting Information

ABSTRACT: The fundamental building blocks of digital electronics are logic gates which must be capable of cascading such that more complex logic functions can be realized. Here we demonstrate integrated graphene complementary inverters which operate with the same input and output voltage logic levels, thus allowing cascading. We obtain signal matching under ambient conditions with inverters fabricated from wafer-scale graphene grown by chemical vapor deposition (CVD). Monolayer graphene was incorporated in self-aligned field-effect transistors in which the top gate overlaps with the source and drain contacts. This results in full-channel gating and leads to the highest low-frequency voltage gain reported so far in top-gated CVD graphene devices operating in air ambient, $A_v \sim -5$. Such gain enabled logic inverters with the same voltage swing of 0.56 V at their input and output. Graphene inverters could find their way in realistic applications where high-speed operation is desired but power dissipation is not a concern, similar to emitter-coupled logic.



KEYWORDS: *Graphene, integrated circuit, logic gates, voltage gain, digital electronics*

The high mobility of charge carriers in graphene[1] at room temperature[2−4] makes this two-dimensional material attractive for applications in high-speed electronics.[5,6] However, graphene field-effect transistors (FETs) must exhibit intrinsic voltage gain $A = g_m/g_d > 1$ in order to be useful in practical electronic applications, where g_m is transconductance and g_d is output conductance. The intrinsic voltage gain of such FETs is limited by the zero bandgap of graphene which prevents depletion of charge carriers. This limits the control of gate voltage over the drain current; i.e., it reduces the transconductance g_m with respect to conventional semiconductor FETs which can be turned off at suitable gate biases.[7] Lack of depletion also leads to a weaker drain current saturation regime in graphene FETs, which in turn increases their output conductance g_d. Hence, most graphene FETs fabricated so far have intrinsic gain smaller than unity,[8−14] preventing the realization of analogue voltage amplifiers and digital logic gates which are the main building blocks of analogue and digital electronics, respectively. Without voltage gain, the use of graphene FETs is limited to niche applications such as analogue mixers,[15] but even these require voltage amplifiers for signal processing. Recent reports of over-unity voltage gain in graphene FETs at room temperature[16−18] pave the way for the use of graphene FETs in analogue electronics. However, such voltage gain has not been utilized so far in digital logic gates at room temperature in which high gain is required in order to match input and output digital signals. Without in/out digital signal matching logic gates cannot be cascaded, and thus realistic digital circuits cannot be realized. Signal matching in graphene inverters has only been reported so far at cryogenic temperatures in exfoliated graphene samples.[19,20]

In this work we demonstrate the highest low-frequency voltage gain obtained so far in wafer-scale graphene integrated circuits under ambient conditions. This voltage gain arises from the large intrinsic gain of the graphene FETs which were integrated into digital complementary inverters. In contrast to other graphene FET implementations in which there were ungated parts of channel on either side of the gate,[21] the FETs described here do not have these ungated parts of the channel due to a self-aligned top-gate fabrication process.[17] Such a scheme results in higher transconductance ($g_m \sim 150\ \mu S/\mu m$) in the fabricated FETs, comparable to that obtained in

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exfoliated graphene FETs deposited on exfoliated hexagonal-BN (h-BN) flakes, which is not a scalable technology.[22] Our top-gated approach also screens the charge traps surrounding the channel and eliminates hysteresis in the transfer curves of the fabricated FETs, which in the past has been detrimental to the stability of graphene devices operating at room temperature.[20,23] In this way we have realized the first integrated wafer-scale graphene logic gates operating with digital signal matching in air ambient at room temperature. We also demonstrate cascading of digital graphene inverters with the previous stage capable of triggering the next stage, which has not been demonstrated so far at any temperature. The combination of transistor properties along with the use of very thin gate insulators employed here results in voltage gains that can be utilized in a large variety of electronic circuits, including analogue voltage amplifiers and digital logic gates.

Integrated graphene complementary inverters were fabricated from graphene monolayers (see Methods section and Supporting Information Figure S1) grown by chemical-vapor deposition (CVD) on Cu with a CH_4 precursor[24] and then transferred to conventional SiO_2(300 nm)/Si substrates. Al gate electrodes were fabricated by direct evaporation of Al on graphene. A very thin (~4 nm) gate insulator (AlO_x) was naturally formed at the interface between the Al gate and graphene by exposing the samples to air.[19] The source and drain contacts (Ti/Au) fabricated in the following step were slightly overlapped with the gate contact in order to completely cover the source-drain channel with the AlO_x/Al gate stack. This maximizes the gate voltage control over the drain current because there are no ungated parts of the channel to add access resistances and reduce the intrinsic voltage gain. As the gate fully covers the channel, the graphene is partially screened from water charge traps adsorbed on the substrate[13,25] such that gate hysteresis is suppressed.[26] The gate also serves as an additional heat sink allowing high drain currents[27] and consequently higher voltage gain. This also reduces the influence of atmospheric contaminants during high-current operation[9,28] such that the electrical properties of the FETs are stable. The AlO_x layer which forms on the surface of the Al gate prevents short circuits between the top gate and the source/drain contacts (despite overlap, gate leakage was found to be negligible; see Methods section).

A schematic of the investigated complementary inverters is shown in Figure 1. As fabricated, both FETs F1 and F2 in each inverter are identical. Examined channel lengths were L = 1 or 2 μm, and other dimensions and details are given in the Methods section. The two FETs change into complementary types (F2 into p-type and F1 into n-type) after the supply voltage $V_{DD} > 0$ is applied.[19] Under bias, the potential of the graphene channel in F2 increases with respect to that of F1, which therefore shifts the Dirac point of F2 to higher input voltages. Complementary operation is obtained between the Dirac points of the two FETs.[9] The highest voltage gain is reached at the direct-current (DC) operating point that lies approximately halfway between the Dirac points of the two FETs.[9,17,19,20] For this reason, the DC components of the input and output voltages at the highest-gain point in inverters biased with negligibly small V_{DD} are $V_{IN} = V_0$ and $V_{OUT} = 0$, where V_0 is the voltage at the Dirac point of the unbiased FETs. As the supply voltage V_{DD} is increased, these two DC components shift by $V_{DD}/(1 + \alpha)$ to $V_{IN} \approx V_0 + V_{DD}/(1 + \alpha)$ and $V_{OUT} = V_{DD}/(1 + \alpha)$ due to circuit symmetry. Here α is the ratio of transistor resistances at $V_{IN} = 0$ (typically $\alpha = 1$).[9] Hence, $V_{IN} - V_{OUT} = V_0$ represents a

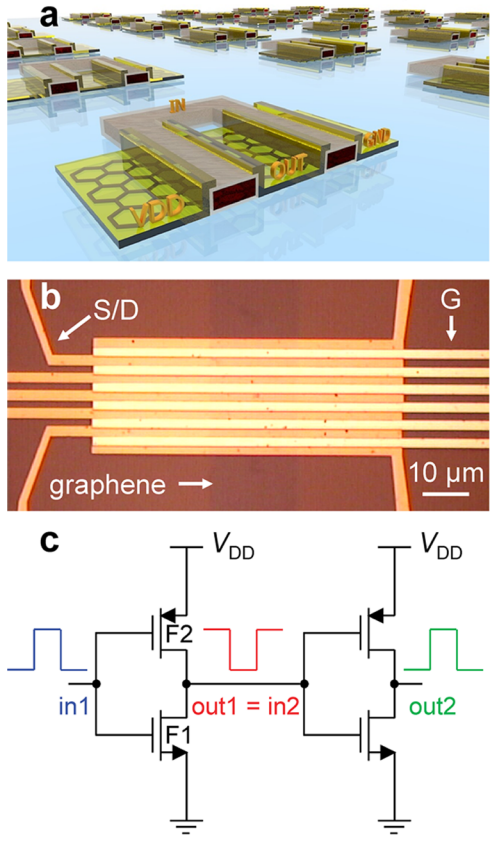

Figure 1. Integrated graphene complementary inverters. (a) A schematic of a large array of inverters fabricated on wafer-scale graphene. Source (V_{DD}, GND) and drain (OUT) contacts (Ti/Au; yellow) overlap with gate (IN) contacts (Al; red core) covered by an insulating layer (AlO_x; gray shell). (b) An optical microscope image of three inverters integrated on the same monolayer graphene channel grown by CVD. The arrows indicate source (S), drain (D), gate (G), and graphene channel. (c) A circuit diagram of two cascaded inverters. The output (out1) of the first inverter (comprised of FETs F1 and F2) is connected to the input (in2) of the second inverter. The test results of cascading two such inverters are shown in Figure 4.

mismatch between the DC components of the input and output voltages at the highest-gain point. This is illustrated in Figure 2, which shows measured alternating current (AC) input and output signals of an inverter biased at the highest-gain point for V_{DD} = 2.5 V. The signals are offset by $V_0 \approx 0.11$ V. A positive voltage V_0 at the Dirac point was found in all fabricated FETs in air (see Figure S2), and it stems from p-type doping introduced by ambient impurities adsorbed on graphene prior to fabrication.[1,29] In addition, we note that V_0 is stable in air at room temperature without hysteresis present,[26] which confirms the good quality of the devices and the protective effect of the top gate.

In the complementary configuration, the DC voltage gain $A_{v,DC} = dV_{OUT}/dV_{IN}$ of an inverter is equal to the intrinsic gain of a single FET,[17] i.e., $A_{v,DC} = -A$. The low-frequency small-signal AC voltage gain $A_v = v_{out}/v_{in}$ was found to be identical to the DC voltage gain, thus demonstrating suppression of the hysteretic behavior of the graphene FETs in air.[17] Here v_{in} and v_{out} are AC components of the input and output voltage signals, respectively. The largest value of the AC voltage gain in air was found to be $A_v = -5.3$ at V_{DD} = 2.5 V (see Figure S4). Over-unity voltage gain is a prerequisite for signal matching;

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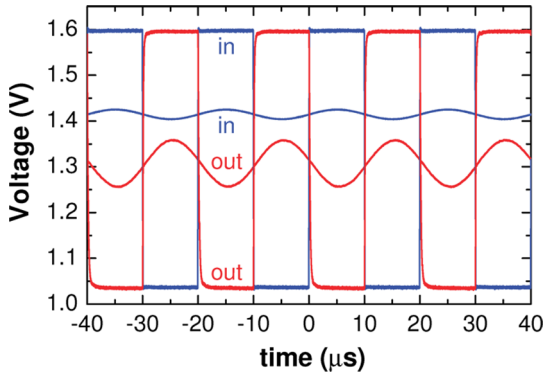

Figure 2. Analogue and digital waveforms measured at the input and output of a typical graphene inverter under ambient conditions at a voltage supply V_{DD} = 2.5 V and frequency f = 50 kHz. Sine waveform signals were measured at the highest-gain point at which there is a mismatch of V_0 = 0.11 V between the DC components of the signals. The amplitude of the output sine wave is 4.7 times larger than the amplitude of the input sine wave; hence A_v = −4.7. Digital waveforms were measured at the DC operating point at which there is no in/out DC signal mismatch. The largest input voltage swing $V_{in,p-p}$ = 0.56 V at which the signals are matched is used. The digital voltage swing is slightly less than in the case when the inverters are operated at the highest gain point ($V_{in,p-p}$ = 0.60 V, see Figure S10).

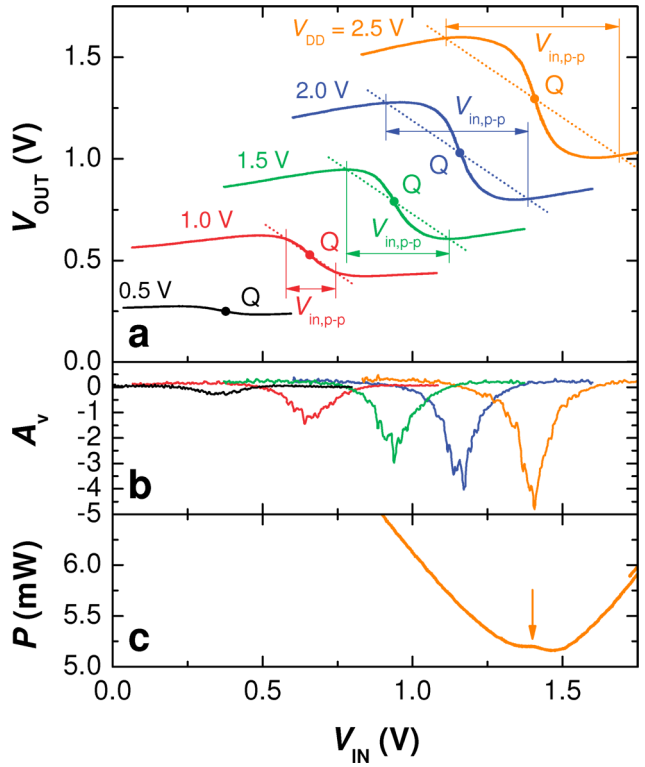

Figure 3. DC characteristics of a graphene inverter under ambient conditions. (a) Transfer curves of an inverter at different supply voltages. The highest-gain point at each supply voltage is denoted by Q. The maximum input voltage swing $V_{in,p-p}$ at which input and output signals are matched ($V_{out,p-p}$ = $V_{in,p-p}$) is determined by the intersections between the transfer curve and a unity gain line (slope of −1) passing through Q. (b) DC voltage gain A_v of the same inverter at different supply voltages. (c) Power dissipation of the same graphene inverter at V_{DD} = 2.5 V. The arrow represents the local maximum of dissipated power at the Q point (see (a) and text), similar to Si inverter technology.

otherwise, the voltage swing at the output is smaller than at the input. The good voltage gain is obtained here in the fabricated FETs due to a combination of factors including full-channel gating, thin gate oxide (leading to good control of the top-gate over the channel), good mobility, low output conductance, and manageable contact resistance (for the ∼1 μm channel lengths explored here). Nevertheless, we note that all of the above can continue to be optimized, yielding further improvements of graphene inverters and amplifiers in future work.

In particular, the top-gated approach employed here results in good transconductance g_m ∼ 3 mS (150 μS/μm) and relatively low output conductance g_d ∼ 1 mS (50 μS/μm) under operating conditions, which leads to A ∼ 3 (see Figure S5). The obtained transconductance is comparable to that measured in exfoliated graphene FETs deposited on very smooth exfoliated h-BN flakes[22] due to the elimination of access resistances through the self-aligned fabrication process.[17] The intrinsic carrier mobility is μ_{in} ∼ 1000 cm^2 V^{-1} s^{-1} after extraction of contact resistance (see Figure S6), which is comparable to carrier mobilities obtained in similar exfoliated top-gated FETs.[19,22] The voltage gain A_v is larger than the intrinsic gain A as the former is measured in an inverter configuration in which the contact resistance of the common drain (i.e., integrated output, see Figure 1) does not influence the measurements. This is because the output of the inverter is loaded with a very large input resistance of a voltmeter, oscilloscope, or next inverter stage. The voltage gain obtained in this work is larger than that of −1.7 recently demonstrated in CVD-grown graphene incorporating interdigitated FETs[16] and also larger than −3.7 obtained in exfoliated samples incorporating FETs similar to those investigated here.[17]

Measurements were performed on inverters in which the Dirac point was close to zero (V_0 < 0.2 V) and which were stable operating with matched signals in air ambient (we have also measured a few devices with initial V_0 > 0.2 V, which required some vacuum exposure to reduce V_0; see Figures S7−S9 and surrounding text). Figure 3a shows the DC transfer curves V_{OUT} vs V_{IN} of one of the inverters at different supply voltages V_{DD}. The voltage gain increases at greater supply voltages[20,17] and the largest value under ambient conditions was typically found to be A_v ∼ −5 at V_{DD} = 2.5 V (Figure 3b). The highest-gain operating point Q is located at V_{IN} ≈ V_{OUT} which allows in/out signals to be matched. As digital signals must have two well distinguished logic states (Boolean 0 and 1) the voltage gain must be >1 if peak-to-peak values (or swing) of the input ($V_{in,p-p}$) and output ($V_{out,p-p}$) digital voltage signals are to be the same. The maximum swing $V_{in,p-p}$ at which $V_{out,p-p}$ = $V_{in,p-p}$ can be determined from the intersection between the transfer curve and a unity-gain line passing through the highest-gain point Q (Figure 3). This exemplifies the importance of a large voltage gain at Q (i.e., large supply V_{DD}), as when this is not satisfied[23] $V_{in,p-p}$ is too small to be reliably detected (i.e., it is below the thermal voltage $V_T = k_BT/e$, where k_B is the Boltzmann constant, T temperature, and e elementary charge). In addition, if devices with V_0 > 0.2 V are used, then biasing inverters away from the highest-gain point Q in order to match in/out signals rapidly reduces the swing $V_{in,p-p}$ (see Figure S7).

Figure 3c shows power dissipation of an inverter as a function of the input voltage. At the highest-gain point Q there is a small local maximum (marked by an arrow) of the dissipated power. In conventional Si inverters this is a global

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maximum of power,[30] and the power reduces to zero on either side of the operating point Q as Si inverters approach rail-to-rail operation, which eliminates static dissipation. The power dissipated by the graphene inverters also decreases on either side of the point Q, but it does not reach zero; instead, the minima are at ≈98% of the local maximum, and thus graphene inverters dissipate power regardless of the position of the operating point. At larger input voltage swings, the power increases as the operating point exits the area between the Dirac points of the FETs and enters the area in which both FETs are highly conductive. The power dissipation could be lowered by reducing the supply voltage V_{DD}. However, this also reduces the voltage gain and consequently $V_{in,p-p}$. Nevertheless, such graphene inverters could find uses in applications not suitable for traditional Si logic, such as transparent circuits on flexible substrates, or ultrafast logic applications where power dissipation is not a concern, further discussed below.

Figure 2 also shows input and output digital voltage signals of an inverter biased with V_{DD} = 2.5 V at an input signal frequency f = 50 kHz. The output signal takes the same logic voltage levels as the input signal, thus allowing inverters to be cascaded which is a key prerequisite in digital electronics. At this supply voltage, the maximum in/out voltage swing is $V_{out,p-p} = V_{in,p-p}$ = 0.56 V or nearly 22 times the thermal voltage V_T, which is large enough for logic states to be unambiguously resolved from one another by the next logic gate. However, graphene FETs cannot be turned off in either of the two logic states, and the in/out voltage swing is only ∼22.4% of the supply voltage. Although this is less than the voltage swing in traditional (e.g., Si-based) complementary metal oxide semiconductor (CMOS) logic (capable of rail-to-rail operation with the voltage swing reaching almost 100% of the supply voltage),[30] it is still more than the swing in emitter coupled logic (ECL) gates, the fastest logic family.[30] Similar to graphene logic gates, ECL gates are also comprised of overdriven transistors in order to achieve ultrafast operation. For this reason a typical swing of the ECL gates is 0.8 V at a supply of 5.2 V, i.e., only 15% of the supply voltage.[30] Static power consumption of a standard ECL gate is ∼10 mW, similar to the consumption of the graphene logic gates. ECL gates are at the core of the fastest SiGe bipolar-CMOS (BiCMOS) or InP heterojunction bipolar transistor (HBT) chips and are used for digital signal processing at extremely high frequencies (EHFs; f > 100 GHz) which are inaccessible with conventional state-of-the-art CMOS technology. For example, they are used in high-speed integer arithmetic units,[31] static EHF dividers,[32] high data rate (>50 Gb/s) serial communication systems for demultiplexing,[33] and phase detection for clock and data signal recovery.[34,35]

Graphene logic gates are expected to offer several advantages over state-of-the-art ECL gates. They are simpler to fabricate than ECL gates as the latter are comprised of complex HBTs. Graphene also has higher charge carrier mobility compared to that of SiGe and InP, which opens a route to higher operating frequencies. Finally, graphene logic is not expected to be constrained by a tradeoff between the highest operating frequency and the breakdown voltage, which represents a serious limitation of HBTs.[36] However, there are also several technological challenges that must be overcome before graphene FETs could replace HBTs in ECL-like logic. Contact resistance of graphene FETs must be reduced to <10 Ω·μm in order to fully exploit the high intrinsic carrier mobility in graphene.[37,38] Graphene FETs are yet to exhibit over-unity voltage gain in the EHF range—the widest reported bandwidth of graphene voltage amplifiers is 6 GHz.[16] Finally, HBT technology provides a simple and flexible route to application-tailored transistors via bandgap engineering. Conversely, bandgap engineering in graphene is mostly limited to patterning graphene into nanoribbons,[39,40] which despite the demonstration of several nanoelectronic prototypes[13,27,41−45] has not yet produced FETs with A > 1.

Demonstration of in/out signal matching does not necessarily imply successful cascading of graphene inverters in realistic applications. Because of remaining fabrication challenges of graphene, two randomly selected inverters usually do not have identical transfer characteristics, i.e., their highest-gain operating points Q1 and Q2 are not the same. As a consequence, it is not possible to bias two inverters such that both of them operate at their highest-gain points. However, we found that a mismatch in the positions of the highest gain points can be compensated if the gain of the inverters is large enough (typically $|A_v| > 3$), which leads to successful cascading. Figure 4 shows input and output voltage signals of two inverters, where the first inverter (1) clocks the second one (2); i.e., the output of inverter 1 is connected to the input of inverter 2 as shown in Figure 1c. The signal matching in Figure 4 was obtained at the DC operating point which lies between the highest-gain points Q1 and Q2 of the two inverters. As both inverters exhibit high gain (here $|A_v| > 4$) at their points Q1 and Q2, they preserve the over-unity voltage gain between these two points, and consequently the gain was maintained on making the cascade connection, resulting in the same logic states 0 and 1 of all signals shown in Figure 4. The final low (high) logic state is correctly interpreted as 0 (1) because its voltage level is below (above) the voltage level of the same state at the input. Such small mismatches between the voltage levels in graphene inverters are expected because the saturation voltage levels in graphene inverters are not well-defined (in contrast to CMOS inverters in which saturation levels are unambiguously defined by ground and V_{DD}). However, this does not influence operation of the cascaded graphene logic gates, as high gain prevents the appearance of intermediate voltage levels (between the high and low levels set by the input) during the propagation of the digital signal.

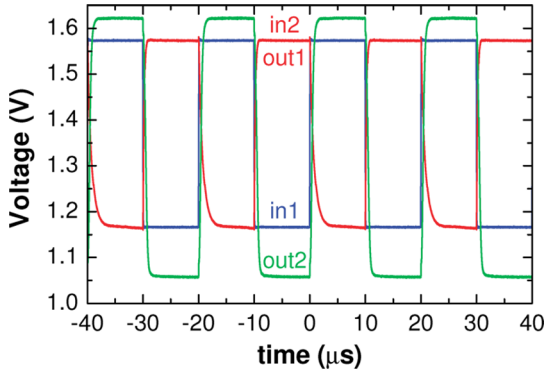

Figure 4. Digital waveforms measured under ambient conditions in a cascade connection of two graphene inverters (connected as in Figure 1c). The supply voltage is V_{DD} = 2.5 V and frequency f = 50 kHz. Transient behavior observed in this plot (see also Figure S14) is a consequence of the limited bandwidth of the used equipment (see Figure S13), as discussed in the Methods section.

In summary, we have demonstrated integrated graphene complementary inverters with matched input and output digital

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signals in room temperature, air-ambient conditions. We have also successfully cascaded graphene logic gates into more complex logic circuits. We realized signal matching with the highest AC voltage gain of ∼−5 reported to date in top-gated graphene FETs from wafer-scale CVD growth. These achievements suggest opportunities for graphene[46] as ultrafast logic gates in scenarios where static power dissipation is not a concern, similar to ECL logic; our graphene logic gates already have larger voltage swing (as a fraction of supply voltage) than ECL gates, and this could be improved through further advances. Importantly, our study has also served to highlight several remaining challenges of graphene FETs, most technological rather than fundamental in nature. For instance, graphene circuits remain sensitive to fabrication-induced variability, but we show that this does not influence the operation of graphene logic gates as long as the graphene FETs exhibit high voltage gain. Finally, achieving higher transconductance (g_m), lower output conductance (g_d), and lower contact resistance will all continue to increase the voltage gain for both analog and digital applications.

Methods. The devices were patterned by electron-beam lithography and reactive-ion etching, while the contacts were deposited in an electron-beam evaporator. Source and drain contacts consisted of Ti/Au (5/35 nm or 2/35 nm) while gate was made of Al (90 nm). FETs with thinner Ti adhesion layers exhibited lower contact resistances and thus higher voltage gain. A ∼4 nm thin gate insulator (AlO_x) was naturally formed at the surfaces of Al by exposing the samples to air.[19,20] Under operating conditions the gate current I_G was found to be less than 1 nA, i.e., at least 6 orders of magnitude smaller than the drain current I_D (see Figures S11 and S12). Gate oxide breakdown occurred at gate voltages V_G > 3 V. After breakdown the resistance between the gate and source/drain contacts was reduced to ∼100 Ω. However, in contrast to previous reports,[19,20] the breakdown was found to be irreversible, probably indicating damage in the overlap area between the contacts. The FET channel dimensions were length L = 2 μm and width W = 20 μm. Apart from these, several devices with L = 1 μm and 500 nm were also fabricated. The voltage gain was found to be independent of L, which was expected as g_m and g_d both scale with W/L.[20,17] All measurements were performed at room temperature in air with the Si substrate grounded. The DC characteristics were measured using Keithley source meters (2611) and multimeters (2000) controlled by a custom-built LabView routine. The waveform measurements were performed by applying input voltages from a Tektronix AFG 3022B function generator while input and output signals were measured by an Agilent Infiniium DSO9064A digital storage oscilloscope. Although fabricated devices have intrinsic unity-gain frequency of ∼9 GHz,[17] the waveform measurements were performed at f = 50 kHz because the bandwidth of the used measurement setup was limited by the output resistance of the inverters (∼1 kΩ) and parasitic capacitance of the cables (∼0.6 nF) to ∼270 kHz (see Figure S13). Measurements performed at higher frequencies are shown in Figure S14.

■ ASSOCIATED CONTENT

Supporting Information

Measurements and discussions on Raman spectrum of monolayer graphene, statistics on the fabricated graphene FETs, transfer curves of the typical graphene FETs, AC signals demonstrating voltage gain A_v = −5.3, typical small-signal parameters of the fabricated FETs in air, statistics on the extrinsic mobility of the fabricated graphene FETs, waveforms measured in samples with larger Dirac voltages at a low pressure, digital waveforms measured in air at the highest-gain point, comparison between drain and gate currents under operating conditions, frequency response of the inverters, and digital waveforms measured at higher frequencies. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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