Graphene Audio Voltage Amplifier

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The main building block of analogue electronics is a voltage amplifier: an electronic device capable of amplifying small alternating current (AC) voltage signals. Many graphene[1] analogue electronic devices performing different functions[2–7] have recently been proposed, stemming from high carrier mobility[8–10] and ambipolar transport in graphene field-effect transistors (FETs). However, none of these devices was capable of signal amplification, thus ultimately requiring integration with Si transistors for performing this most important task. Here, we demonstrate an integrated graphene voltage amplifier which, together with the recently reported high-frequency graphene voltage amplifier,[11] paves the way for all-graphene analogue electronics. Signal amplification was obtained by fabricating graphene transistors in which the top gate overlaps with the source and drain contacts. This results in full-channel gating and therefore high transconductance at room temperature. The fabricated complementary push–pull amplifier has a voltage gain of 3.7 (11.4 dB) at 10 kHz, a total harmonic distortion in the audio frequency range of <1%, a unity-gain frequency of 360 kHz and a –3 dB bandwidth of 70 kHz (tested limits). The obtained values demonstrate that, among other applications, the present graphene amplifier is suitable for high fidelity amplification of audio signals.

Graphene is emerging as a possible replacement for Si in future nanoelectronic devices. The high mobility of charge carriers in graphene[8–10] allows fabrication of very fast transistors,[12–15] having a potential to overcome state-of-the-art Si and III–V semiconductor-based high-frequency FETs at the ultimate scaling limits.[16] In contrast to Si, carrier transport in graphene is ambipolar, and this allows the same functionalities—such as logic gates,[17] frequency doublers,[2] analogue mixers,[3] and phase modulators[4] and detectors[6,7]—to be realized with fewer FETs. However, graphene does not have a bandgap, which severely limits the extent of current modulation in graphene FETs by electrostatic gating,[18] especially in back-gated devices with thick (≈300 nm) gate insulators. For this reason, the small-signal AC voltage gain $A_v = v_{out}/v_{in}$, where v_{in} and v_{out} are AC components of the input and output voltage signals, is usually much less than unity in graphene circuits. This either results in the inability to directly couple digital logic gates (due to a mismatch between input and output voltage logic levels)[17,19] or to amplify analogue AC signals.[5] Current modulation in graphene devices can be increased by patterning graphene into nanoribbons, which increases the current on/off ratio.[20–22] However this also significantly reduces the on current,[23,24] which in turn reduces voltage gain. Recently it has been shown that a very thin (<4 nm) Al_2O_3 layer naturally forms at the interface between graphene and an Al layer evaporated on top.[25] Such a layer was utilized as a gate insulator in digital graphene devices exhibiting $A_v \approx 15$ dB but only at cryogenic temperatures and without appreciable gain at room temperature.[26] Quite recently, a voltage gain larger than unity was demonstrated at room temperature in a complex 6-finger-gate FET configuration.[11] Despite the relatively small gain (4.5 dB), which was measured on an infinite load in a high-frequency transmission-line environment, this result represents an important step toward graphene amplifier circuits. However, room-temperature operation of general-purpose graphene amplifiers with a high voltage gain (>10 dB) has remained elusive, meaning that graphene analogue circuits should rely on Si FETs for signal amplification,[27] therefore incurring the higher production costs of such a hybrid technology. Here we demonstrate graphene voltage amplifiers capable of high-gain signal amplification on conventional loads at room temperature in a frequency range well exceeding the audio range of 20 kHz.

Audio amplifiers usually consist of two stages.[28] The first stage is a voltage amplifier (the present device, which is also sometimes called a preamplifier) whose purpose is to amplify the input voltage signal (hence voltage gain $|A_v| > 1$). The second stage of every audio amplifier is a power amplifier (with a unity voltage gain) whose sole purpose is to match the previously amplified signal (provided by the voltage amplifier) to a low-impedance load (≈4 Ω) such as a loudspeaker. Audio voltage amplifiers need to have a very low noise figure in order to provide high fidelity reproduction. Graphene FETs are well suited as building blocks of low-noise amplifiers as they exhibit very low levels of the electronic flicker noise (or $1/f$ noise, where f is the frequency) which dominates

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the noise spectrum in the audio frequency range.[29–31] Such voltage amplifiers are also expected to benefit from high mechanical and chemical stability and high thermal conductivity of graphene.[32]

In order to investigate the electrical properties of graphene voltage amplifiers, graphene FETs were fabricated by exfoliating monolayer graphene from highly ordered pyrolytic graphite on conventional SiO_2/Si substrates. The complete graphene channel between the source and drain contacts (Ti/Au) is covered with an Al_2O_3/Al gate stack (**Figure 1**a,b) which was fabricated by direct evaporation of Al. Source (S), drain (D), and gate (G) contacts were patterned by e-beam lithography. Complete channel coverage

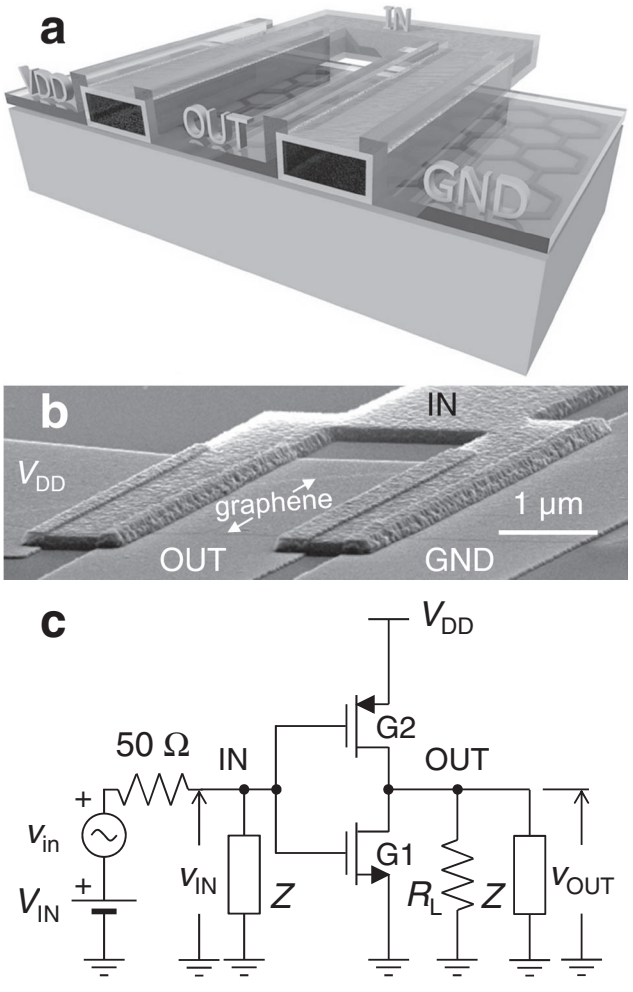

Figure 1. Integrated graphene voltage amplifier. a) A schematic of an amplifier. Source (supply, V_{DD}, and ground, GND) and drain (output, OUT) contacts (Ti/Au) overlap with gate (input, IN) contacts (Al; dark core) covered by an insulating layer (Al_2O_3; bright shell). b) A tilted scanning electron microscope image of a device. The arrows indicate the extent of the graphene flake. c) A circuit diagram of the amplifier. Z = 1 MΩ □ 13 pF is the input impedance of the oscilloscope used to measure input and output signals while 50 Ω is the output resistance of the input voltage source. Since $|Z| >> 50\ \Omega$ the input signal fully drops across Z, i.e., $v_{IN}(t) = V_{IN} + v_{in}(t)$, where V_{IN} is the DC bias voltage and $v_{in}(t)$ is the AC component of the input signal. The amplifier is additionally loaded with R_L which simulates the input resistance of the next amplifying stage. This resistance was either infinite, 30 kΩ, or 10 kΩ, depending on the measurement.

was obtained by overlapping the source/drain contacts with the gate contact, which was fabricated first. A similar full-channel coverage exists in conventional Si metal oxide–semiconductor FETs[33] and allows maximum drain current modulation as there are no ungated parts of the channel that contribute to fixed series resistances which reduce the voltage gain. The Al_2O_3 layer which forms on the surface of the Al gate prevents short circuits between the contacts. The gate also serves as an additional heat sink which allows high drain currents I_D and consequently high voltage gain A_v. Additionally, as the gate fully covers the channel, desorption of adsorbates from graphene is suppressed at high drain currents,[19,34] and therefore the electrical properties of FETs are stable during operation.

Voltage amplifiers were realized both in a complementary push-pull[35] (Figure 1c) and resistive-load (Supporting Information (SI), Section S1) configuration. As fabricated, both FETs G1 and G2 in a complementary amplifier are identical (SI, Section S2). On application of the supply voltage $V_{DD} > 0$ the potential of the graphene channel in G2 increases with respect to that of G1, which therefore shifts the Dirac point of G2 to higher input voltages.[25] Complementary operation is obtained between the Dirac points of the two FETs, where the increase in input voltage V_{IN} causes the resistance R_2 of G2 to increase and the resistance R_1 of G1 to decrease.[19] This results in a large rate of decrease of the output voltage $V_{OUT} = V_{DD}/(1 + R_2/R_1)$ as the input voltage V_{IN} is increased, and doubles the voltage gain A_v with respect to a resistive-load amplifier in which G2 is replaced by a fixed resistor (SI, Section S1). The complementary amplifier is considered to be integrated since FET G2 loads FET G1, and both are integrated on the same graphene flake, i.e., the amplifier does not require any additional load for signal amplification. The only external components are those which supply the voltages V_{IN} and V_{DD}. The additional load R_L shown in Figure 1c is not part of the amplifier: it is introduced in order to demonstrate how the amplifier would operate if it were loaded with the next (i.e., power) amplifying stage (R_L represents an input resistance of this amplifying stage). Finally, 50 Ω is the output resistance of the input voltage source and is not needed for amplifier operation.

Figure 2a shows the transfer curve V_{OUT} vs. V_{IN} of the amplifier for V_{DD} = 1.5 V. The largest value of the voltage gain $|A_v|_{max}$ = 2.1 for this supply voltage is obtained at the direct-current (DC) operating point Q (Figure 2b). The dependence of the maximum voltage gain on the DC circuit parameters can be derived from the expression for the low-frequency voltage gain $A_v = dV_{OUT}/dV_{IN} = -g_m r_d$ where $g_m = \partial I_D/\partial V_{GS}$ and $r_d = \partial V_{DS}/\partial I_D$ are the transconductance and output resistance of the FETs (SI, Section S3). Hence $|A_v|_{max} = V_{DD}/(\Delta V_{IN} + 2\sigma_0 t_{ox}/(\varepsilon_{ox}\mu))$ where ΔV_{IN} is the input voltage separation of the Dirac points of the transistors, σ_0 is the conductance of the graphene channels at the Dirac point, t_{ox} and ε_{ox} are the thickness and dielectric constant of the gate oxide and μ is the mobility of charge carriers in graphene. This shows that higher gain can be achieved at higher supply voltages (i.e., higher drain currents), which was experimentally confirmed (SI, Section S3). The transconductance of fabricated FETs at high supply voltages is $g_m/w \approx 0.5$ mS μm^{-1}, where w is the

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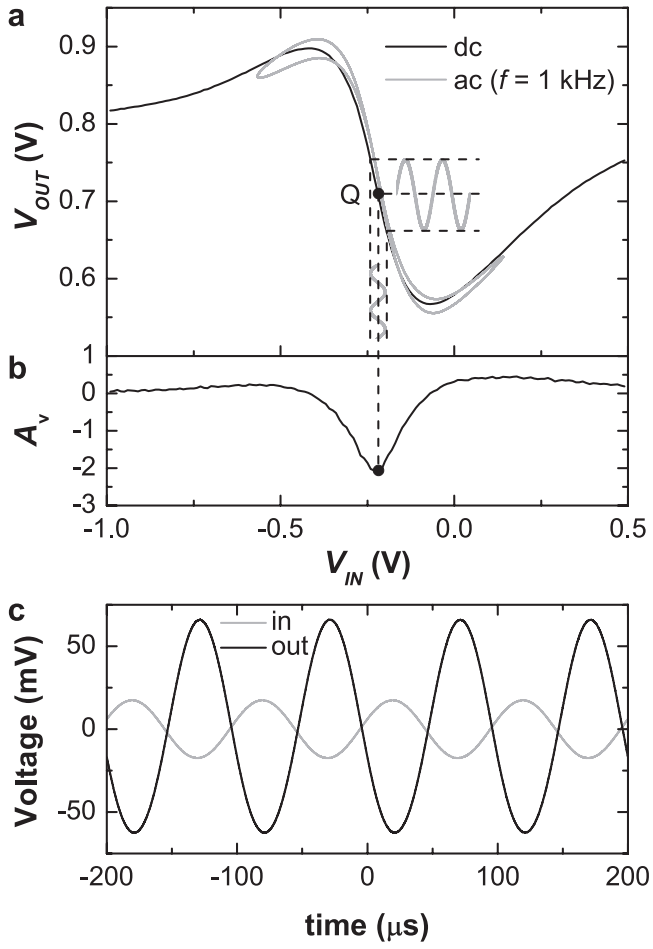

Figure 2. Voltage amplification. a) Static (DC) transfer curve V_{IN} vs. V_{OUT} of the amplifier is shown in black. Dynamic (AC) transfer curve is shown in gray and was obtained by plotting output voltage v_{OUT} vs. input voltage $v_{IN} = V_{IN} + V_{in}\sin(2\pi f t)$, where $V_{IN} = -0.22$ V, $V_{in} = 0.35$ V and $f =$ 1 kHz. Hysteretic behavior in the dynamic mode can only be observed at the ends of the curve, and is due to parasitic reactive components in the circuit rather than hysteretic behavior of the graphene FETs. Both DC and AC curves were measured for $V_{DD} = 1.5$ V and $R_L \rightarrow \infty$. b) Low-frequency voltage gain $A_v = dV_{OUT}/dV_{IN}$. To achieve maximum amplification the amplifier should be biased at the operating point Q ($V_{IN,Q} = -0.22$ V, $V_{OUT,Q} = 0.71$ V) at which $|A_v|$ has a maximum $|A_v|_{max} = 2.1$. If a small AC signal is applied on top of $V_{IN,Q}$ at the input then the AC signal at the output will have $|A_v|_{max}$ times larger amplitude (these signals are shown in gray in (a)). c) AC components of the input and output voltage signals at a frequency $f = 10$ kHz for $V_{DD} = 2.5$ V and $R_L \rightarrow \infty$. The voltage gain is $A_v = -3.7$. The DC components of the signals are $V_{IN} = 0.15$ V and $V_{OUT} = 1.15$ V.

width of the FET channel. Such transconductance combined with relatively large output resistance r_d $w \approx 10.5$ kΩ μm (due to the quasi-saturation of drain current, see SI, Section S4) results in measured voltage gains above 10 dB.

Figure 2c shows measured AC components of the input and output voltage signals of the amplifier biased at $V_{DD} = 2.5$ V. At this supply voltage a maximum voltage gain $|A_v|_{max} = 3.7$ was measured at an input frequency f of 10 kHz. The drain current density at the DC operating point Q is $I_D/w \approx 0.26$ mA μm^{-1}, which is about 5 times smaller than the breakdown current density of exfoliated graphene.[36] Such a current density and additional heat dissipation into the top gate means that even higher gain could be obtained at higher supply voltages without risking damage to the graphene channels. However, this was not attempted as the upper part of the graphene channel in G2 is at the potential V_{DD}, resulting in a potential drop of V_{DD}–V_{IN} across the gate oxide in this area. For $V_{DD} >$ 2.5 V this potential drop is >2.35 V, which may be enough to cause oxide breakdown (SI, Section S5). Signals shown in Figure 2c confirm that high voltage gain is preserved in AC mode, which is attributed to the absence of gate hysteresis (see also Figure 2a) due to the full-channel coverage by the gate which partially screens water charge traps adsorbed on the substrate.[24,37] As the output resistance of the amplifier is not very large ($r_d/2 \approx 1.8$ kΩ), high voltage gain will also be preserved if the output of the amplifier is loaded with a resistance >18 kΩ (see SI, Section S6 for signal amplification under additional loads $R_L = 10$ or 30 kΩ). This eliminates the stringent requirement for the input resistance of the next amplifying stage, which otherwise would have to be very large in order to eliminate signal attenuation due to the voltage dropped over the output resistance of the amplifier.

The frequency response of the fabricated amplifier in the frequency range $f < 5$ MHz is shown in **Figure 3**. The amplifier is biased at $V_{DD} = 2.5$ V which gives the maximum signal amplification $|A_v|_{max} = 3.7$ (11.4 dB). This gain is preserved at very low frequencies due to a direct coupling both at the input and output of the amplifier (i.e., there is no lower cut-off frequency). The gain remains constant up to about 20 kHz, and then decreases as the frequency is increased, dropping by 3 dB at the higher cut-off frequency $f_{-3\ dB} =$

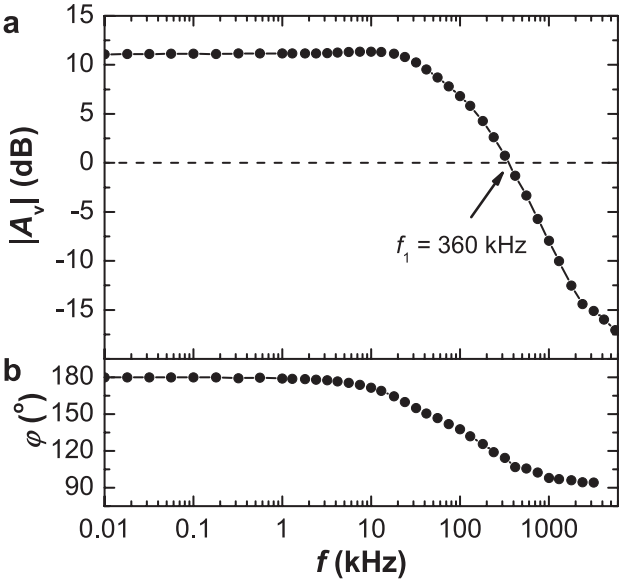

Figure 3. Frequency response $A_v = |A_v| \angle\phi$ of the amplifier for $V_{DD} =$ 2.5 V and $R_L \rightarrow \infty$. a) Magnitude $|A_v(f)|$ of the voltage gain. The magnitude decreases at 18 dB dec^{-1} at high frequencies, which is very close to the decrease of 20 dB dec^{-1} expected from a dominant pole at $f_{-3\ dB}$. b) Phase shift ϕ (f) between output and input signals introduced by the amplifier. The frequency response at lower supply voltages is shown in SI, Section S3.

70 kHz which also defines the bandwidth of the amplifier. The amplifier is capable of signal amplification up to a unity-gain frequency f_1 = 360 kHz. At this frequency, the amplifier operates as a unity-gain amplifier (buffer), while for $f > f_1$ it attenuates the input signal. The signal phase shift ϕ introduced by the amplifier is 180° at low frequencies (signal inversion), decreasing to 90° at high frequencies. Both amplitude and phase characteristics of the voltage gain indicate a typical dominant-pole (at $f_{-3\ dB}$) behavior. However, this pole does not originate from the amplifier but from the capacitances of the cables used to connect the amplifier to the measurement equipment. The cables were found to have a total conductor-to-ground capacitance $C_c \approx 0.5$ nF which results in a pole frequency $f_p = (2\pi\ (r_d/2+R_c)\ C_c)^{-1} \approx 100$ kHz, where R_c is the contact resistance of the output line (SI, Section S7). The obtained value coincides with the measured cut-off frequency $f_{-3\ dB}$. As no other poles were observed, the fabricated amplifier has cut-off and unity-gain frequencies above 5 MHz which may extend its application also to high-frequency circuits (an intrinsic unity-gain frequency can be estimated to be ≈9 GHz, SI, Section S7).

For most applications, especially regarding the amplification of audio signals, it is necessary that the amplifier operates in a linear mode, i.e., that it does not introduce noticable harmonic distortion. **Figure 4** shows a power spectrum of the output signal in the audio frequency range (f < 20 kHz) when the input is a sinusoidal test signal at a frequency f_0 = 1 kHz. Nonlinearity of the amplifier results in the generation of higher harmonics at frequencies $f = nf_0$, $2 \le n \le 20$. The harmonic distortion of the fabricated amplifier is mostly dominated by the second and third harmonic, whereas the second harmonic is 42 dBm below the first harmonic. As a measure of nonlinearity, the total harmonic distortion (THD) was calculated as a square root of the total output power of all higher harmonics divided by the power of the first harmonic.[38] The data shown in Figure 4 result in THD = 0.999%, demonstrating the high-fidelity reproduction of the amplifier at low input signal amplitudes.[38] As the amplitude V_{in} of the input signal is increased, nonlinearity in the transfer curve increases the total harmonic distortion which reaches 17.5% at a clipping input signal amplitude of 160 mV (the output signal is clipped when the operating point reaches the maximum and minimum in the transfer curve, at which the voltage gain drops to zero). Although THD > 3% is audible,[38] the harmonic distortion level as a function of input signal is a more important figure of merit for power amplifiers (which operate with large input amplitudes) rather than of voltage amplifiers (which operate with small input amplitudes). In contrast to Si complementary amplifiers in which the clipped peak-to-peak output voltage reaches almost 100% of the supply voltage, here this value is only 22% of the supply voltage due to the inability to turn off graphene FETs. Si amplifiers also exhibit larger gains, typically >20 dB.[39]

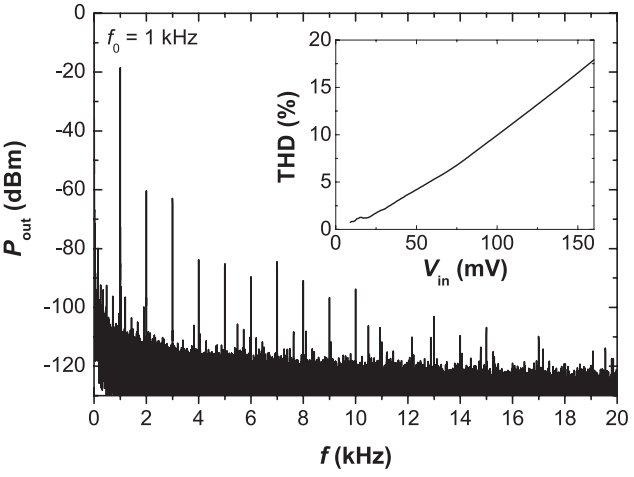

Figure 4. Power spectrum of the output signal when the input is a sinusoidal test signal at a frequency f_0 = 1 kHz and amplitude V_{in} = 18 mV. Inset: total harmonic distortion as a function of the input signal amplitude. Circuit parameters are V_{DD} = 1.5 V and $R_L \to \infty$.

In summary, we have fabricated graphene voltage amplifiers based on graphene FETs in which the complete graphene channel is covered by an Al_2O_3/Al gate stack. This results in large intrinsic gain of fabricated FETs at room temperature, which was exploited to realize voltage amplifiers in complementary push-pull and common-source configurations. The complementary amplifier has a voltage gain of 11.4 dB and a –3 dB frequency response up to 70 kHz, with a unity-gain frequency of 360 kHz. Even higher gains could be obtained with higher supply voltages, with the use of gate dielectrics with higher breakdown voltages. The amplifier has a total harmonic distortion of <1% suggesting a possible use of the amplifier in high-fidelity amplification of audio signals. This result represents an important step toward simple, general-purpose high voltage gain graphene amplifiers which could serve as the main building block of all-graphene analogue electronics.

Experimental Section

Graphene flakes were exfoliated by a standard Scotch-tape method[1] on SiO_2/Si substrates with a back gate. Optical microscopy, atomic force microscopy and Raman spectroscopy[40] were used to identify monolayer flakes (SI, Section S8). Exfoliated graphene was used as this is the material of highest quality, which served to estimate the upper performance limits of the fabricated graphene amplifiers. The devices were patterned by an e-beam lithography while the contacts were deposited in an e-beam evaporator. Source and drain contacts consisted of Ti/Au (5/35 nm) while gate was made of Al (≈100 nm). A 4 nm-thin gate insulator (Al_2O_3) was naturally formed at the surface of Al by exposing the samples to air.[25,26] Typical FET channel dimensions are length ≈1 μm and width ≈3 μm. We found that fabricating the contacts in the correct order was essential in obtaining reproducible results. If the source/drain contacts were made first the yield of working devices was very low (≈5%). However, by fabricating the gate contact first the yield of working devices was considerably higher (≈50%). We attribute this yield asymmetry to the very large thermal expansion coefficient of Al, which has one of the largest thermal coefficients of all metals, e.g., almost three times that of Ti.[41] Almost all of the working devices (≈90%) exhibited signal amplification ($|A_v| > 1$), however only smaller number of them (<20%) exhibited high–gain signal amplification. High-gain devices were found to be those with almost identical transistors G1 and G2 (i.e., with identical/symmetric transfer curves I_D vs. V_G) and capable

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of withstanding large supply voltages (V_{DD} > 2 V) without appreciable leakage currents (I_G < 1 nA). All measurements were performed at room temperature with the back gate grounded. The DC characteristics were measured by Keithley sourcemeters (2611) and multimeters (2000) controlled by a custom-built Labview routine. The AC measurements were performed by applying input AC/DC voltages from a Tektronix AFG 3022B function generator while input and output signals were measured by an Agilent infiniium 54832D mixed-signal oscilloscope.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author. This section includes measurements and discussions on resistive load amplifiers, transistor symmetry in a complementary configuration, voltage gain in a complementary configuration, current–voltage characteristics of a single graphene transistor, gate breakdown characteristics, complementary inverter with a finite load, high-frequency operation, and Raman spectra.

Acknowledgements

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