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Gate-controlled rectifying barrier in a two-dimensional hole gas

R Sordan, A Miranda, J Osmond, D Colombo, D Chrastina, G Isella and H von Känel

L-NESS, Dipartimento di Fisica del Politecnico di Milano, Via Anzani 42, I-22100 Como, Italy

E-mail: roman.sordan@como.polimi.it

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Abstract

The current flowing in a homogeneous low-dimensional conductor is shown to be rectified by a gate-controlled asymmetric barrier resembling a Schottky barrier. The barrier shape is set by varying the potential along a nanofabricated nonequipotential gate which allows simple external control over the device function independent of material properties. A forward-to-reverse current ratio of more than 10^4 is obtained. The merits of diodes fabricated in this way with respect to conventional diodes are discussed.

1. Introduction

The emergence of novel low-dimensional systems, such as carbon nanotubes [1] and graphene [2], has sparked great interest in their possible incorporation in future electronic devices [3, 4]. The research on these systems has mainly been focused on field effect transistors (FETs) [5, 6], yet many conventional applications cannot be realized without diodes [7–9]. To this end, p–n junctions have been fabricated by chemical [10] or electrostatic [11] doping. In the former case the shape of the rectifying barrier is predetermined by the fabrication process, while in the latter case the barrier can be externally controlled by gates. The use of gate-induced junctions opens a route to reconfigurable electronic devices and provides valuable insight into the understanding of low-dimensional nanostructures. Flexible external control over the barrier shape allows easy probing of their fundamental properties and enables fabrication of p–n junctions [12] even in cases where chemical doping is challenging [13, 14]. Here we demonstrate that similar research may be permitted in a unipolar regime, where an asymmetric barrier reminiscent of a rectifying Schottky barrier is induced by a gate. The method is based on the use of a nanofabricated nonequipotential gate and can be applied to any type of nanostructure exhibiting the field effect, regardless of its dimensionality. The principle is illustrated here by demonstrating a diode functionality in an otherwise homogeneous two-dimensional hole gas (2DHG) confined in a quantum well (QW).

Nonequipotential gates [15] have attracted only limited interest so far. They have been used either to improve linearity of the FET channel resistance in the triode regime [16] or to eliminate the need for submicrometre interelectrode gaps in charge-coupled devices [17]. Recently, a very long ($\sim$500 μm) resistive gate was used in the observation of a large excitonic mobility in coupled GaAs QWs [18]. The inhomogeneous potential [19] induced by such a gate could also be used to fabricate a unipolar version of a bipolar junction transistor or to induce a spin polarized current in a nanostructure [20].

2. Device structure

The device structure is shown in figure 1(a). The diode was fabricated by patterning a SiGe modulation doped heterostructure grown by low-energy plasma-enhanced chemical vapour deposition [22]. The heterostructure consists of a $Si_{0.3}Ge_{0.7}$ graded virtual substrate [23] with a 16 nm thick strained-Ge QW located 83 nm below the top surface. Holes in the QW form a 2DHG and originate from a boron doped delta layer which is positioned 40 nm below the QW and therefore does not screen the gate. Heterostructures with low-temperature hole mobility $\mu_p \sim 40\,000$ cm^2 V^{-1} s^{-1} at sheet density of $p_s \sim 4 \times 10^{11}$ cm^{-2} were used [24]. A metal gate is patterned on top of the heterostructure. A potential V_G is applied to one end of the gate, the other end of which is grounded (with a current $I_{G\|} \sim 2$ μA flowing along the gate under nominal conditions). This creates an asymmetric barrier to holes in the QW, as shown in figure 2. It is the in-plane hole current I (flowing parallel to the gate in the homogeneous QW

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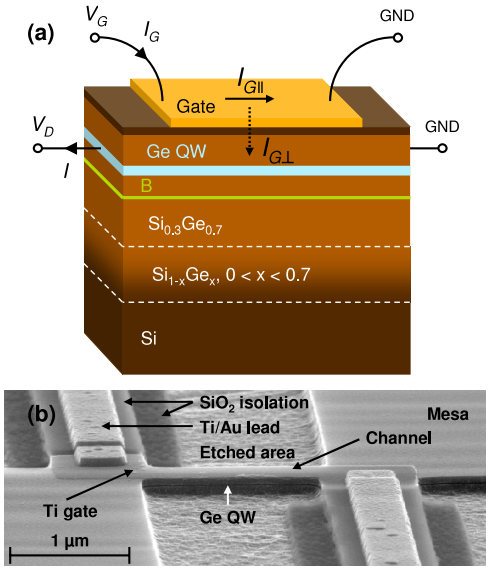

Figure 1. A reconfigurable diode utilizing a nonequipotential gate. (a) A schematic of the device, showing the nonequipotential gate over a strained-Ge QW grown on a graded virtual substrate. (b) Scanning electron microscope image of the nanofabricated diode. A 2 μm long and 1 μm wide channel was defined by reactive ion etching. The Ge has been etched faster than the surrounding $Si_{0.3}Ge_{0.7}$, so the location of the Ge QW can be identified by a dark narrow slit 83 nm below the top surface. A 70 nm thick SiO_2 isolation layer was patterned below the leads in order to suppress the leakage current [21].

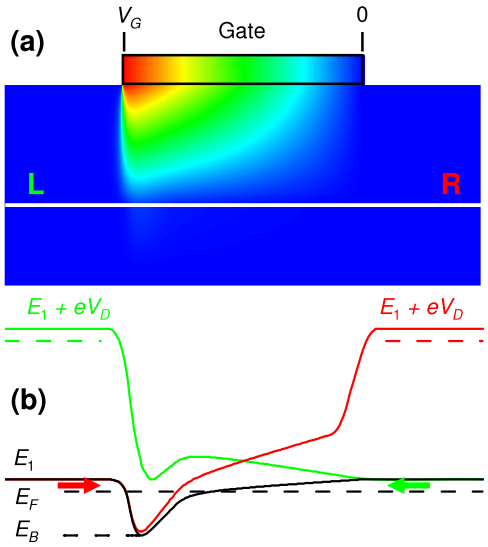

Figure 2. Model for rectification in a device with a nonequipotential gate. (a) Potential distribution along the gate and calculated potential induced by the gate inside the semiconductor (the cross section is 4 μm × 150 nm). (b) Potential energy distribution for holes inside the QW (white line in the upper image) at zero drain bias (solid black line) and at a negative drain potential when the drain contact is on the left (L, solid green line) and right side (R, solid red line) of the QW. E_B is the energy of the barrier maximum, E_F is the Fermi level, and E_1 is the bottom energy of the lowest subband in the QW. At the hole sheet density of 4×10^{11} cm^{-2}, $E_F - E_1 \sim 9.5$ meV. The direction of the electrical current under drain bias is marked by arrows in corresponding colours. The electrostatic potential in the absence of drain bias was calculated by solving the discrete Poisson equation assuming no current in the semiconductor. It was qualitatively assumed that most of the applied drain bias drops at the drain–gate edge (because the electric potential in the channel is significantly influenced by the gate which is not screened by the doping layer), while the rest is distributed linearly along the channel [28, 29].

when a negative drain potential V_D is applied) which is rectified by the induced barrier, rather than the gate leakage current $I_{G\perp}$ flowing across the gate contact as in a conventional nano-Schottky diode [25, 26]. The hole current is rectified solely by the induced barrier if the gate leakage current $I_{G\perp}$ is negligible, i.e., when the gate current I_G is equal to $I_{G\parallel}$. In our case a reverse-biased Schottky contact is used, but the asymmetric barrier would be present even if the gate and nanostructure were insulated by a dielectric layer.

The complete structure was fabricated in seven lithography steps, and is shown in figure 1(b). The voltage drop at the gate electrode was obtained by contacting the gate with two leads, each at one side. In order to supply potentials V_G and zero from an external voltage source to the gate while minimizing voltage drop along the leads, the gate was fabricated from a very thin (8 nm) Ti layer which has a resistance much higher than that of the thick Ti(20 nm)/Au(100 nm) leads.

3. Principle of operation

An asymmetric potential barrier resembling a rectifying Schottky barrier is implemented by a gradually biased gate electrode, as shown in figure 2. When the left-hand side of the gate electrode is held at a positive potential V_G and the right-hand side is grounded, then the potential of the gate electrode linearly decreases from left to right. Such a potential drop forms an asymmetric quasi-triangular potential barrier in the nanostructure below the gate and gradually depletes the holes in the QW (assuming a p-type well). If a negative drain potential V_D is applied to the left-hand side of the QW shown in figure 2 (herein the source is always at the opposite side and grounded) then the barrier is efficiently lowered at the drain side. By making the drain potential more negative, more holes are injected over the barrier from the source and the forward drain current strongly increases. If the drain and source are interchanged, a negative drain bias has little influence on the barrier height (which is now at the source side) and the reverse drain current is suppressed. The suppression is stronger at higher gate voltages when the barrier is higher. Drain-induced barrier lowering is responsible for the main component of the subthreshold current in a standard short-channel FET [27]. Unlike the nonequipotential gate, the gate in a standard FET forms a symmetric barrier which makes the subthreshold current symmetric with respect to the exchange of drain and source contacts.

All measurements were carried out at 30 K. At higher temperatures, more carriers are expected to overcome the rectifying barrier and thus suppress the rectification effect. Rectification could be preserved by increasing the gate voltage V_G which increases the barrier height. Room temperature operation was not possible to test as the temperature range was restricted due to material limitations. Above 50 K there is background conduction through the $Si_{0.3}Ge_{0.7}$ virtual substrate

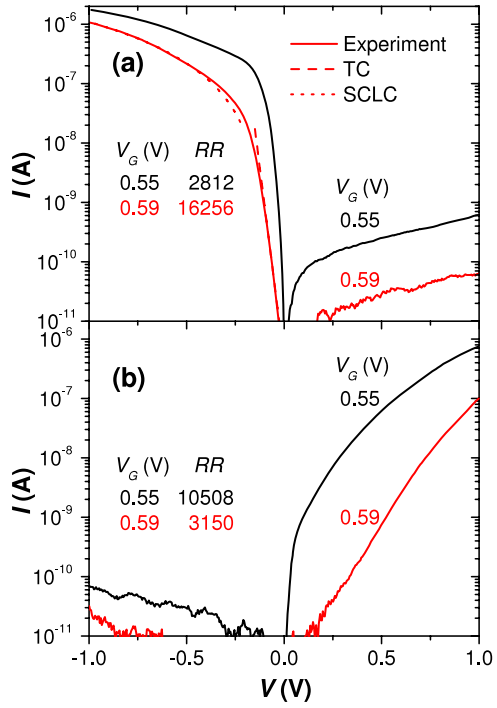

Figure 3. Measured current–voltage characteristics of the nanofabricated diode shown in figure 1(b). Voltage V_G is applied on the left side of the gate electrode (as in figure 2) in (a) and on the right side in (b). In both cases, negative voltage V corresponds to a negative drain voltage V_D applied on the left side ($V = V_D$), while positive voltage V corresponds to a negative drain voltage V_D applied on the right side ($V = |V_D|$). Large (forward) current is obtained when the drain contact is at the side of the gate electrode which is at the potential V_G. Fits to a thermionic (TC, dashed line) and space–charge limited current (SCLC, dotted line) are shown in (a) for the case of the best rectification.

(This figure is in colour only in the electronic version)

in addition to a gate leakage current $I_{G\perp}$ typical for Schottky contacts in alloys with high Ge content. The gate leakage could be suppressed by using a gate insulator without affecting the working principle of the device. Below 10 K the samples exhibited a strong hysteretic quenching of the electrical current at small drain biases, usual for the low-temperature operation of Ge junction FETs [30]; correct assessment of the diode function requires that the reverse current is suppressed only by the asymmetric potential barrier.

4. Results and discussion

Measured current–voltage characteristics of a nanofabricated diode are shown in figure 3. The first set of measurements (figure 3(a)) was performed by applying a potential V_G to the left side of the gate while keeping the right side grounded, as in figure 2. Rectification was achieved by increasing V_G above 0.5 V, at which point the potential barrier inside the QW became large enough to suppress the reverse current efficiently. A large (forward) current was obtained when the drain contact was on the left, while a small (reverse) current was obtained when the drain contact was on the right (in agreement with figure 2). In order to assess the quality of the diode, the rectification ratio RR was defined as the ratio of forward and reverse currents at a magnitude of the drain voltage of 1 V. The best RR of 1.6×10^4 was obtained at $V_G = 0.59$ V. When the gate biasing was swapped (left side grounded and right side biased at V_G), the rectification effect was also swapped (figure 3(b)), i.e., the forward current was obtained when the drain contact was at the opposite side with respect to the previous case. In this configuration, RR $= 1.1 \times 10^4$ was obtained at a gate potential of $V_G = 0.55$ V. In both cases, it was possible to obtain arbitrary values of RR between 1 and the maximum value simply by tuning the gate voltage. At higher gate voltages, RR was found to decrease due to a suppression of the forward current by a higher barrier. In that case, a more negative drain voltage was needed to reach the maximum RR.

Control measurements were performed in order to exclude gate leakage current $I_{G\perp}$ (negligible at 30 K) and Coulomb drag [31] (caused by the current flowing along the gate) as possible sources of current rectification. Regarding possible rectification from unintentional asymmetry in the structure of the device or contacts, we found that there was negligible rectification effect when both ends of the gate were biased to the same V_G. Furthermore, the drain voltage was measured in a four-point probe configuration. All contacts were verified to be ohmic in the temperature range studied. Charged traps at the gate/semiconductor interface could possibly explain a small variation (usually about 5%) in the gate voltage at which maximum rectification ratio is obtained in repeated measurements of the same samples. Interfacial charges were not found to have an influence on overall device characteristics. As in a conventional diode, the diode fabricated here rectifies the current when an alternating voltage is applied to one side (the right-hand electrode in figure 2), in which case the rectification is additionally enhanced (RR $= 6.7 \times 10^5$) by a circuit-induced asymmetry [32].

The charge transport in the samples investigated here can be explained in terms of thermionic and space–charge limited emission, while the tunnelling current is expected to be negligible due to the smooth and wide profile of the potential barrier. The forward current consists mostly of holes injected over the barrier from the source. At low magnitudes of drain voltage, the dominant transport mechanism is thermionic emission with the forward current given by [28] $I = I_S \exp[|V_D|/(nV_T)]$, where I_S is the saturation current, $n \geqslant 1$ the ideality factor, $|V_D|/n$ the fraction of the applied forward bias $|V_D|$ lowering the barrier, and $V_T = k_B T/q$ the thermal voltage (k_B is the Boltzmann constant and q the elementary charge). In the case of the highest rectification ratio obtained (for $V_G = 0.59$ V in figure 3(a)) the values are $I_S = 2.3$ pA and $n = 6.5$. Such a large ideality factor (which is 1 for an ideal diode) is a consequence of the position of the barrier maximum which is not at the drain–gate edge, but moved toward the source (figure 2). A similar conclusion can also be drawn from the expression relating the ideality factor of a conventional Schottky diode to the position of the barrier maximum [33]. As a result, the barrier is lowered by an amount less than $|V_D|$ because the potential in the channel is more strongly influenced by the gate [29]. This also explains why the ideality factor is larger at larger gate voltages. From the value

of the saturation current the barrier height in figure 2 can be estimated to be [34] $E_B - E_1 = 47$ meV. When the magnitude of the drain voltage reaches $\sim n(E_B - E_F)/q = 240$ mV, the barrier maximum coincides with the Fermi level in the source. At that point, the density of holes injected into the barrier region exceeds the low density of background ionized impurities in the channel [35] and opposes further barrier lowering due to a space–charge effect [36]. As a consequence, for larger magnitudes of drain voltage the current can be fitted to a square law $I = B(|V_D| - V_0)^2$, where $B = 1.3\ \mu AV^{-2}$ and $V_0 = 95$ mV for the highest RR obtained. Fits to thermionic and space–charge limited current are shown in figure 3(a).

The main advantage of the proposed concept is the possibility of externally inducing a rectifying barrier of desired height. Such external control over a device function seems very attractive, though other factors should be considered in estimating a figure of merit. The presently fabricated diode dissipates 1 μW of static power due to a potential drop at the gate electrode. The gate power consumption can be minimized by increasing the resistance of the gate electrode (e.g., by using thinner films) or by replacing the nonequipotential gate with multiple equipotential gates. In both cases, the diode will have more than two terminals, making its use in conventional applications cumbersome. Finally, room temperature operation has yet to be demonstrated. This would require modification of the fabrication procedure to use gate insulators. Such a modification would also be necessary if the method were to be applied to carbon nanotubes [37] and graphene [12]. It would not however be required when applied to CdS nanowires [38].

5. Conclusion

We have presented a simple example of barrier engineering resulting in an asymmetric rectifying barrier in a 2DHG and associated diode operation. The concept is based on nanofabricated nonequipotential gates, does not require any material inhomogeneity in the direction of current flow, and can be applied to a wide range of fast unipolar nanostructures made from diverse materials. Although conventional applications of diodes fabricated in this way are limited by power consumption and the number of terminals, their use could provide new insight into understanding the properties of low-dimensional systems.

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