Integrated complementary graphene inverter

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The operation of a digital logic inverter consisting of one *p*- and one *n*-type graphene transistor integrated on the same sheet of monolayer graphene is demonstrated. Both transistors initially exhibited *p*-type behavior at low gate voltages, since air contamination shifted their Dirac points from zero to a positive gate voltage. Contaminants in one transistor were removed by electrical annealing, which shifted its Dirac point back and therefore restored *n*-type behavior. Boolean inversion is obtained by operating the transistors between their Dirac points. The fabricated inverter represents an important step toward the development of digital integrated circuits on graphene. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3148342]

Graphene, a recently isolated[1] single sheet of graphite, is currently being investigated as a viable alternative to Si for the channel of field-effect transistors (FETs) at the sub-10-nm scale, at which the ultimate limits of Si technology would probably be reached.[2] The high mobility of carriers in graphene[3,4] could allow fabrication of FETs with a very low channel resistance, resulting in a high operational speed.[5] The remarkable electronic properties of graphene[6] and its compatibility with Si lithographic techniques[7,8] promise to simplify the transition to carbon-based electronics.[9] Large-scale fabrication of graphene, which is currently being attempted by epitaxial growth,[10,11] transfer printing,[12–14] or deposition from a solution[15] is the following step in the development of graphene-based integrated circuits. However, only single-transistor operation[16–18] has been demonstrated so far. Here we demonstrate the operation of the first graphene integrated electronic circuit, consisting of two graphene FETs of opposite types. The transistors are fabricated on the same sheet of monolayer graphene and comprise an integrated digital logic inverter (NOT gate), the main building block of Si complementary metal-oxide-semiconductor (CMOS) digital electronics.[19]

The fabricated inverter is schematically depicted in Fig. 1. Graphene flakes were deposited by mechanical exfoliation of highly oriented pyrolitic graphite on a highly doped Si substrate with 300 nm of thermally grown dry SiO_2 on top.[1] A metal contact evaporated on the back of the Si substrate was used as a back gate. The inverter was fabricated on a flake, which was identified as a monolayer graphene by Raman spectroscopy.[20] The flake was contacted by three Cr(5 nm)/Au(50 nm) electrodes patterned by e-beam lithography. Each part of the flake contacted by a pair of neighboring electrodes (source and drain contacts) comprises a channel of one of the two graphene FETs, which share the same back-gate used as voltage input (IN). Both FETs show identical *p*-type behavior at small gate voltages, which has been attributed to hole-doping by physisorbed ambient impurities, such as water[1] and oxygen.[21] The measured transfer resistance R_p between the source and drain contacts of one of the FETs [the right-hand one in Fig. 1(a)] as a function of the applied back-gate voltage V_{IN} is shown in Fig. 2. The *p*-type behavior is exhibited up to the Dirac point (resistance maximum), which is reached at $V_{IN}=13.9$ V. For higher input voltages, the Fermi level crosses into the conduction band resulting in type inversion.

In order to fabricate an inverter, one of the transistors [the left-hand one in Fig. 1(a)] was electrically annealed[22] to shift its Dirac point to lower input voltages. Annealing was carried out in a He atmosphere (~5 mbar) at $T=3$ K and $V_{IN}=0$ V. The source-drain voltage was increased from zero to 3 V in steps of 0.1 V to remove ambient contamination by Joule heating. After each step, the voltage was held constant for ~5 min. The highest drain current reached was ~350 μA. For voltages larger than 2.5 V, the drain current

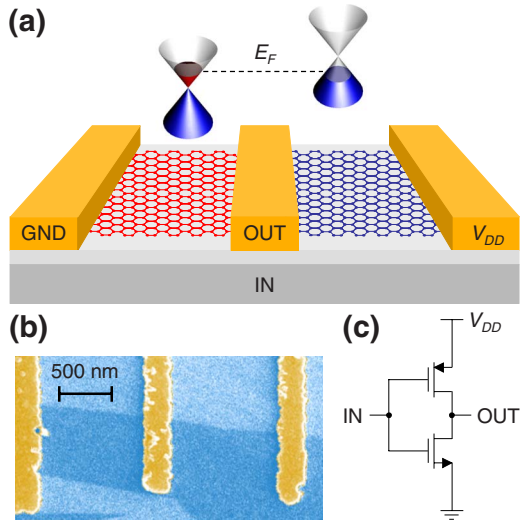

FIG. 1. (Color online) Integrated complementary graphene inverter. (a) A schematic of the fabricated inverter. Three electrodes patterned on the same flake of monolayer graphene define two FETs. The part of the flake between the two leftmost electrodes (depicted in red) is electrically annealed to obtain an *n*-type FET. The other part of the flake (depicted in blue) is a pristine *p*-type FET. The flake is electrically insulated from the input (highly doped Si depicted in dark gray) by a layer of SiO_2 (depicted in bright gray). (b) Scanning electron microscopy image of the fabricated inverter. Electrode separation (channel length) is 1 μm. (c) The circuit layout (power supply $V_{DD}=3.3$ V).

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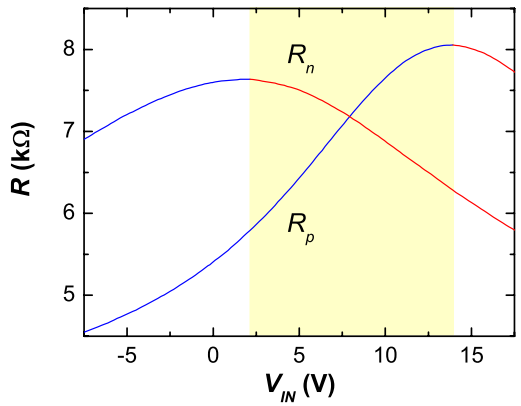

FIG. 2. (Color online) Resistance curves R vs V_{IN} of the graphene transistors schematically depicted in Fig. 1 at $T=3$ K. The curve denoted by R_n (R_p) corresponds to the left (right) transistor. Segments of the curves displaying n-type (p-type) behavior are drawn in red (blue). In the range (shaded in yellow) between Dirac points ($2.1\ \text{V} < V_{IN} < 13.9\ \text{V}$) transistors exhibit complementary behavior, i.e., the Fermi level in the left (right) transistor is in the conduction (valence) band, as depicted in Fig. 1(a).

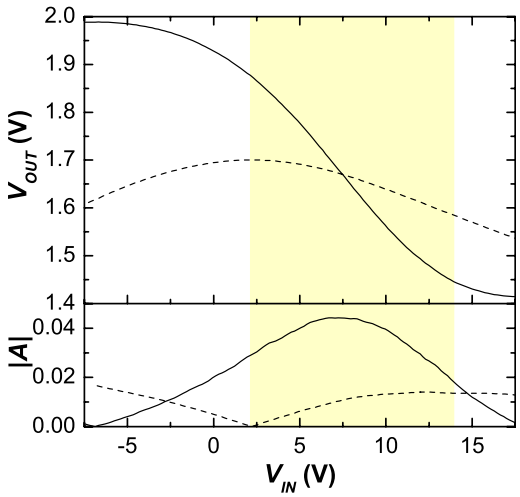

FIG. 3. (Color online) The measured dc voltage transfer characteristics of the fabricated complementary graphene inverter (solid lines) and a resistive-load inverter (dashed lines) obtained by replacing the p-type transistor by a resistor. The characteristics are represented by the output voltage V_{OUT} and absolute value of the voltage gain $A=dV_{OUT}/dV_{IN}$ as functions of the input voltage V_{IN} at $T=3$ K. The FETs exhibit complementary mode of operation in the range shaded in yellow.

noticeably decreased during the hold time due to the removal of p-type impurities. After annealing, the resistance curve of the annealed transistor R_n versus V_{IN} was found to be shifted to lower input voltages with the peak at $V_{IN}=2.1$ V, as shown in Fig. 2. The annealing procedure did not affect the other transistor, whose resistance curve R_p versus V_{IN} (also shown in Fig. 2) was unchanged. Hence, the transistors exhibit complementary behavior (nonannealed as a p- and annealed as an n-type FET) in the range $2.1\ \text{V} < V_{IN} < 13.9$ V. Electrical annealing offers a simple way to change the type of a selected transistor, in contrast with conventional thermal annealing,[23] which affects all transistors on a chip.

The inverter was realized by connecting the source of the n-graphene FET to ground (GND), the source of the p-graphene FET to a conventional CMOS supply voltage $V_{DD}=3.3$ V, and the output (OUT) to the common drain of the FETs (Fig. 1).[19] In this configuration, the output voltage is given by $V_{OUT}=V_{DD}/(1+R_p/R_n)$. The measured voltage transfer characteristics of the fabricated inverter are shown in Fig. 3. The transfer curve V_{OUT} versus V_{IN} can be understood from the previous expression and Fig. 2, as the graphene FETs stay in the Ohmic regime even at very large drain biases. They function as simple voltage controlled resistors whose resistances R_p and R_n depend solely on the applied gate voltage V_{IN}. The two FETs operate in the complementary mode between Dirac points. In this range, increase in V_{IN} causes resistance R_p to increase and R_n to decrease, which results in a strong increase in the ratio R_p/R_n. As a consequence, V_{OUT} decreases with the increase in V_{IN} giving rise to the voltage inversion shown in Fig. 3. Away from the Dirac points, the output voltage saturates as both FETs enter the same mode of operation (p-type for $V_{IN} < 2.1$ V and n-type for $V_{IN} > 13.9$ V) making the ratio R_p/R_n approximately constant. However, in contrast with a CMOS inverter, the output voltage does not saturate to zero or V_{DD} as neither of the FETs can be turned off. Inability to turn off the FETs stems from the absence of a band gap in graphene and the formation of electron-hole puddles.[24]

The threshold voltage V_{TH} of a logic gate is usually defined as the input voltage at which the absolute value of the voltage gain $A=dV_{OUT}/dV_{IN}$ (shown in Fig. 3) reaches a maximum. This ensures the maximal output voltage swing, i.e., a clear distinction between Boolean 0 and 1 at the output. The maximum absolute gain of $|A|=0.044$ was reached at $V_{IN}=V_{TH}=7.5$ V (Fig. 3). At this operating point R_n is slightly larger than R_p (the resistance curves in Fig. 2 intersect at $V_{IN} \simeq 8.0$ V), so the output voltage is slightly larger than $V_{DD}/2$. The small voltage gain of the fabricated inverter is due to a very small change in the resistance of the transistors around the Dirac point, i.e., due to the impossibility of turning the transistors off (the resistance off/on ratio in Fig. 2 is only $\simeq 1.8$). Although the small gain also suppresses noise, the logic gates do not have a noise margin as the gain is always less than 1 and there is a mismatch between the input offset V_{TH} and output offset $\simeq V_{DD}/2$ (in contrast with conventional CMOS gates where $V_{TH}=V_{DD}/2$).

Voltage inversion can also be obtained if one of the FETs is replaced by an off-chip resistor.[18] However, in this case the corresponding resistance in the ratio R_p/R_n is constant so the output voltage V_{OUT} decreases more slowly when V_{IN} increases. To demonstrate this, an n-graphene inverter was realized by replacing the p-type transistor with an off-chip resistor of the same resistance at $V_{IN}=7.5$ V. The measured voltage transfer characteristics of such a resistive-load inverter are shown in Fig. 3. The much smaller output voltage swing and gain obtained in this case stress the importance of the complementary mode of operation.

Voltage transfer characteristics are presented at $T=3$ K in order to evaluate the upper limit of performance of the fabricated inverter. The characteristics were also measured at room temperature by keeping the inverter in vacuum ($\sim 10^{-2}$ mbar) so as not to reintroduce ambient contamination which would shift the Dirac point of the annealed transistor back to the original position.[22] The principle of operation did not change at room temperature, but broadening of resistance peaks degraded inverter performance. The output voltage swing was damped and the highest measured absolute value of the voltage gain was $|A|=0.027$. The supply voltage $V_{DD}=3.3$ V was found to be too high for room-temperature operation, since it caused further annealing of

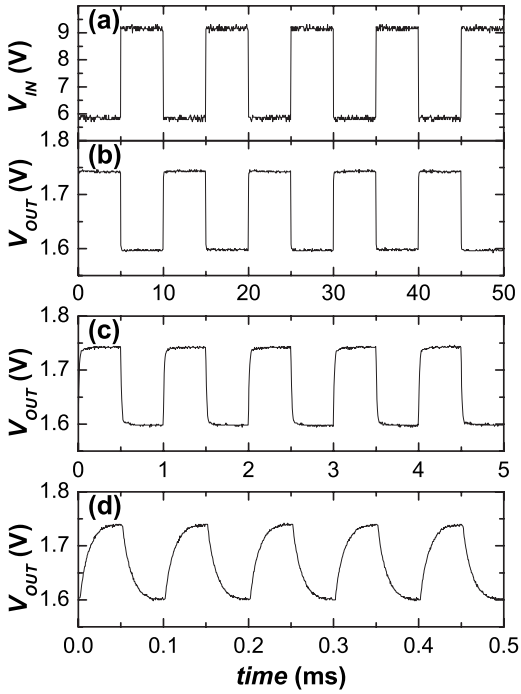

FIG. 4. Digital waveforms measured on the fabricated inverter. (a) Input voltage. The offset is 7.5 V, voltage swing $V_{DD}=3.3$ V, and frequency $f=100$ Hz. The following panels show the output voltage at $T=3$ K with input signal frequency of (b) $f=100$ Hz, (c) $f=1$ kHz, and (d) $f=10$ kHz.

the transistors. At lower supply voltages ($V_{DD}=1.1$ V) the annealing effect was negligible. Instead, the Dirac points were found to slowly shift with time, probably due to contamination of the graphene by residual gasses. In contrast, by keeping the sample at $T=3$ K the position of the peaks did not change in 60 days, although the inverter was repeatedly measured with the full supply voltage of $V_{DD}=3.3$ V.

Dynamic pulse response measurements of the fabricated inverter at three different clock rates of the input signal are shown in Fig. 4. The measurements were performed by driving the inverter with a square-wave signal with the offset $V_{TH}=7.5$ V. The total input voltage swing was $V_{DD}=3.3$ V as in conventional CMOS logic gates. Under these conditions, stable and separated output logic levels are obtained at all frequencies, as shown in Fig. 4. However, the output voltage swing ($\simeq 0.15$ V) is much smaller than the input voltage swing (3.3 V) because of the small voltage gain. As the clock rate of the input signal is increased the output signal becomes more distorted, and already at 10 kHz propagation delay can no longer be neglected. The large total parasitic capacitance $C \simeq 3$ nF of the measurement equipment connected to the output of the inverter and the output resistance of the inverter $R=(R_p^{-1}+R_n^{-1})^{-1} \simeq 3.5$ kΩ limit the clock rate to $f_{max}=1/(2\pi RC) \simeq 15$ kHz. In principle, by loading the output with a typical gate capacitance of $C \sim 10$ fF, a clock rate of $f_{max} \sim 4.5$ GHz could be obtained. Further increase in f_{max} by reduction in length of the graphene FETs (to reduce R by reducing the R_p and R_n) will be hampered by unscalable contact resistance.

Although this inverter seems to be an attractive alternative to a Si CMOS inverter, there are other two important figures of merit that should be considered. First, the inverter is always conducting, i.e., the output stage dissipates a static power $V_{DD}^2/(R_p+R_n) \sim 0.77$ mW, in contrast with a CMOS inverter in which there is no static power dissipation. The static dissipation could be reduced by using graphene transistors with a higher resistance, but this would increase the transient response time making this inverter slower than a state-of-the-art CMOS inverter. Hence, there is a trade-off between the static dissipation and the highest possible clock rate. Second, input and output logic voltage levels are not the same, so the inverters could not be directly cascaded. This problem could be mitigated to some extent by decreasing the input threshold V_{TH} to $V_{DD}/2$ by annealing both transistors. However, this would not increase the voltage gain, so the mismatch between the input and output voltage swing would prevent direct cascading.

In summary, a complementary logic inverter was fabricated by integrating two transistors of the opposite type on the same flake of a monolayer graphene. The voltage transfer characteristics of the fabricated inverter exhibit clear voltage inversion. Dynamic pulse measurements display characteristic NOT functionality when the inverter is operated with a CMOS input voltage swing and supply voltage. Although application of the present inverter is limited by power consumption and inability for direct cascading, its realization demonstrates feasibility of using graphene as a substrate on which complete electronic circuits can be integrated.

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