Exclusive-OR gate with a single carbon nanotube

R. Sordan,[a] K. Balasubramanian, M. Burghard, and K. Kern
Max-Planck-Institut für Festkörperforschung, Heisenbergstr. 1, D-70569 Stuttgart, Germany

(Received 12 August 2005; accepted 13 December 2005; published online 2 February 2006)

Carbon nanotubes (CNTs) are now well-established as efficient channels for field-effect transistors (FETs). Logic circuitry based on CNTs have until now been demonstrated by replacing the silicon channel of a conventional metal-oxide-semiconducutor FET by a CNT. We propose a circuit design utilizing the ambipolarity of the Schottky-barrier-type CNT-FET to realize an exclusive-OR (XOR) gate using a single CNT. The merits and limitations of such a CNT-XOR gate with respect to conventional XOR gates are discussed. © *2006 American Institute of Physics*.
[DOI: 10.1063/1.2171474]

The evergrowing demand for increasing the integration scale of digital electronics has prompted a search for novel devices at the nanometer scale. Field-effect transistors (FETs) made of individual carbon nanotubes (CNTs) have proven to be a promising alternative to silicon-based devices due to their small size and extraordinary performance.[1] Moreover, several logic circuits based on such CNT-FETs have been realized.[2–5] However, in all these cases standard digital circuitry was replicated by simply replacing the $n(p)$-type metal-oxide-semiconductor FETs (MOSFETs) with the $n(p)$-type CNTs. In order to develop CNTs into an attractive replacement for Si devices, it would be important to achieve novel functionalities of the devices, or to implement the same functionality with fewer transistors. Here we propose the latter strategy by utilizing the ambipolarity of CNTs[6,7] to realize an exclusive-OR (XOR) gate from a single CNT transistor. By comparison, the transistor count using MOSFETs for the same logic gate is between 4 and 12, depending on the design.[8,9] On the other hand, using GaAs[10] or Si[11,12] based multigate single electron transistors fabricated in a different device architecture, XOR gates have been realized with just one device. XOR gates are the fundamental building blocks of digital encryption and parity checking electronics.

Under ambient conditions, semiconducting CNTs not subjected to further treatment generally show p-type behavior, which has been attributed to hole doping of the CNTs or the CNT-metal contacts modified by physisorbed oxygen.[13,14] Upon oxygen removal via outgassing in vacuum,[15] the injection of both electrons and holes across the Schottky barriers becomes possible, imparting an ambipolar behavior. Conductance versus back-gate voltage V_G of the investigated outgassed CNT-FET is shown in Fig. 1. The CNT-FET was fabricated by depositing single wall CNTs (obtained from the HiPco process) on a silicon substrate with thermally grown oxide layer and contacting them by ~ 1.3 μm spaced gold–palladium electrodes patterned by e-beam lithography. The p-type behavior of this CNT-FET can be observed between the operating points Q_1 and Q_2. Upon increasing the gate voltage beyond the threshold point Q_2, the n-type regime is reached between the operating points Q_2 and Q_3.

Conduction in the subthreshold region is present also in conventional Si MOSFETs but it is regarded as undesirable. This is due to the large drain voltage needed to bring the transistor to ON state, causing a breakdown of the drain-substrate p-n junction. Breakdown can cause physical damage to the device. Furthermore, the breakdown current cannot be controlled by the gate voltage and the transistor action would be lost. On the other hand, in Schottky-barrier MOSFETs, the current can be carried by both types of carriers and they exhibit ambipolar characteristics.[16] But, in addition to the gate voltage, the drain bias also needs to be inverted to change the type of carriers. By contrast, in the case of CNTs, the ambipolar conduction is symmetric, i.e., the transistor effect is present with both types of carriers at small drain bias with the same polarity.

The existence of symmetric p- and n-type conduction in the CNT device enables the selection of operating points Q_1, Q_2, and Q_3 such that the point Q_2 (with $V_2=13.6$ V) lies exactly half of the voltage range between the points Q_1 (at $V_L=7.2$ V) and Q_3 (at $V_H=20$ V). Points Q_1 and Q_3 exhibit identical high conductance values of $G_H=25.5$ nS, while the point Q_2 has a low conductance value of $G_L=0.188$ nS. The symmetric position of these three operating points can be exploited to design a two-input XOR gate as illustrated in Fig. 2. The input stage is designed such that the gate voltage V_G is an arithmetic mean of the two inputs, i.e., $V_G=(V_{G1}+V_{G2})/2$. Thus, if both input voltages are the same (either at the low state V_L or at the high state V_H), the conductance of

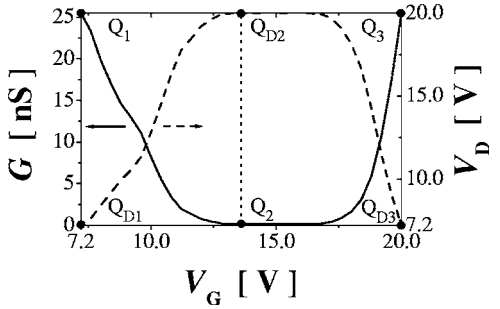

FIG. 1. Room temperature transfer curve $G(V_G)$ of a semiconducting CNT is shown by a solid line. Dashed line depicts the output drain voltage V_D of the same CNT incorporated in electronic circuit shown in Fig. 2. Operating points are: $Q_1(V_L,G_H)$, $Q_2(V_2,G_L)$, $Q_3(V_H,G_H)$, $Q_{D1}(V_L,V_L)$, $Q_{D2}(V_2,V_H)$, and $Q_{D3}(V_H,V_L)$. Values are: $V_L=7.2$ V, $V_H=20$ V, $V_2=(V_L+V_H)/2=13.6$ V, $G_L=0.188$ nS, and $G_H=25.5$ nS.

[a]Author to whom correspondence should be addressed; electronic mail: roman@fkf.mpg.de

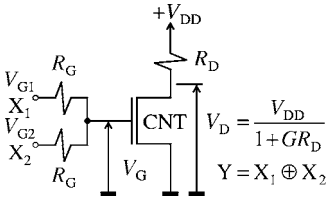

FIG. 2. A two-input (X_1 and X_2) XOR gate incorporating one CNT transistor. The gate voltage is $V_G=(V_{G1}+V_{G2})/2$.

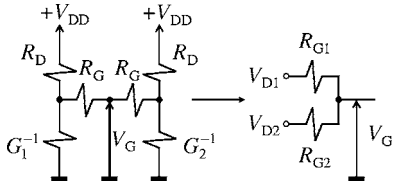

FIG. 3. The input stage of an XOR gate driven by two other identical gates (left), and its Thévenin equivalent (right).

the CNT will be $G=G_H$. On the other hand, if one input voltage is low (V_L) and the other high (V_H), the net gate voltage will be $V_G=V_2$, so that the CNT will be in the low conductance state with $G=G_L$. Using positive logic (boolean 0 corresponding to low, and boolean 1 to high) the conductance G of the CNT is an inverted XOR function of the input voltages V_{G1} and V_{G2}.

In a real digital circuit it is important to utilize logic function at the voltage output of a transistor. For that purpose, the drain contact of the CNT is connected via a pull-up resistor R_D to a supply voltage V_{DD}, which makes a simple voltage divider. The output voltage is then given by $V_D(G)=V_{DD}/(1+GR_D)$. Consequently, the output voltage is low $[V_D=V_{DL}=V_D(G_H)]$ if the input voltages are identical, and high $[V_D=V_{DH}=V_D(G_L)]$ if the input voltages are different, whereby an XOR logic function of inputs is implemented. The complete truth table of this simple circuit is given in Table I, where the logic symbols of voltages V_{G1}, V_{G2}, and V_D are denoted by X_1, X_2, and Y, respectively.

The electronic components R_G, R_D, and V_{DD} of the presented XOR gate should be appropriately designed to allow direct coupling between different gates, which is essential to preserve the main advantage of this logic gate over the MOSFET XOR gate. Without such a direct coupling, additional interface electronics will increase the transistor count. To arrive at the optimal values for these components, the voltage generators V_{G1} and V_{G2} in the input stage of the XOR gate are replaced by the output stages of two other gates. This is shown on the left-hand side of Fig. 3, where G_1 and G_2 represent the conductances of the nanotubes in the other gates. A Thévenin equivalent of this input stage is shown on the right-hand side, where $V_{D1,2}=V_D(G_{1,2})$ denote the output voltages of the two CNT-XOR gates, and $R_{G1,2}=R_G+R_D/(1+G_{1,2}R_D)$. Direct coupling would be possible if the input and output logic voltage levels were the same

$$V_H = V_{DH} \Rightarrow V_H = \frac{V_{DD}}{1 + G_L R_D}$$

$$V_L = V_{DL} \Rightarrow V_L = \frac{V_{DD}}{1 + G_H R_D}$$

and if the input stage in Fig. 3 is symmetric

TABLE I. Truth table of the simple XOR gate shown in Fig. 2.

X_1	X_2	V_{G1}	V_{G2}	V_G	G	V_D	$Y=X_1\oplus X_2$
0	0	V_L	V_L	V_L	G_H	V_{DL}	0
0	1	V_L	V_H	V_2	G_L	V_{DH}	1
1	0	V_H	V_L	V_2	G_L	V_{DH}	1
1	1	V_H	V_H	V_H	G_H	V_{DL}	0

$$R_{G1} = R_{G2}.$$

The first two equations imply the following conditions for R_D and V_{DD}:

$$R_D = \frac{V_H - V_L}{G_H V_L - G_L V_H},$$

$$V_{DD} = \frac{G_H - G_L}{G_H V_L - G_L V_H} V_L V_H,$$

while the third one is satisfied only if $R_G \gg R_D$ for nonidentical conductances of the CNTs ($G_1 \neq G_2$). For the CNT presented in Fig. 1, the values of R_D and V_{DD} are 71.2 MΩ and 20.3 V, while R_G can be taken as $10R_D=712$ MΩ. The output voltage V_D of an XOR gate with the values of the components as chosen above is plotted in Fig. 1. This plot confirms that the output voltages in the operating points Q_{D1}, Q_{D2}, and Q_{D3} indeed correspond to the input voltage levels V_L or V_H.

In the assessment of the merits of the suggested XOR gate, there appear several factors that may limit its performance. First, the CNT gate consumes considerably more power than a complementary metal-oxide-semiconductor (CMOS) gate, because there is current flow in the ON state. The ON current could be eliminated by replacing the pull-up resistor R_D with a complementary CNT, which should be in the OFF state when the bottom CNT is in the ON state, and vice versa. Unfortunately, this task would require a CNT with an inverse transfer characteristic to that shown in Fig. 1, which is impossible using semiconducting CNTs. Second, the high output resistance (in the 10 MΩ range) leads to a large RC time constant making this gate much slower than a CMOS gate, whose output resistance is only in the 10 Ω range. This problem could be mitigated to some extent by using a sample with $G_H \gg G_L$, in addition to having symmetric p- and n-type conduction. While this cannot be achieved with outgassed samples (as in the present case), other devices fabricated using alternative methods[6] and coated with a protective layer indeed show symmetric transfer curves with a large G_H to G_L ratio. Third, the current synthesis procedures do not allow one to obtain CNTs with identical electrical characteristics. A variation in the transport characteristics from one device to another would lead to each XOR gate having different ON and OFF current levels. Depending on the method of fabrication, this variation could be as high as one order of magnitude. Another consequence is that the gate dependence of the conductance will not be uniform from one device to another. Shifts of few volts in the threshold voltage are common in such devices created using present-day fabrication techniques. Since the operating points of one logic gate will broadly differ from that of another, cascading of CNT-XOR gates would be hard to achieve. Finally, as high gate voltages are needed to switch the CNT to the OFF state,

the direct coupling of CNTs remains challenging because they cannot sustain such high drain voltages without causing damage to the carbon framework. Possible solutions to this problem include the use of suspended CNTs[17] or CNT-FETs fabricated with a thin gate oxide[18] or with a gate insulator of high dielectric constant,[5] where the OFF state can be reached at much smaller gate voltages.

In conclusion, we have designed a two-input XOR gate with just a single carbon nanotube, making use of the ambipolar nature of CNT-FETs. Such logic gates can be directly cascaded to each other, thus eliminating a need for interface logic-level shifters. Although this gate is attractive because of its low transistor count, further improvements are required to approach the performance of CMOS XOR gates.

[1]Ph. Avouris, J. Appenzeller, R. Martel, and S. J. Wind, Proc. IEEE **91**, 1772 (2003).
[2]V. Derycke, R. Martel, J. Appenzeller, and Ph. Avouris, Nano Lett. **1**, 453 (2001).
[3]A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, Science **294**, 1317 (2001).
[4]A. Javey, Q. Wang, A. Ural, Y. Li, and H. Dai, Nano Lett. **2**, 929 (2002).
[5]A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. McIntyre, P. McEuen, M. Lundstrom, and H. Dai, Nat. Mater. **1**, 241 (2002).
[6]R. Martel, V. Derycke, C. Lavoie, J. Appenzeller, K. K. Chan, and J. Tersoff, Phys. Rev. Lett. **87**, 256805 (2001).
[7]A. Javey, M. Shim, and H. Dai, Appl. Phys. Lett. **80**, 1064 (2002).
[8]S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits Analysis & Design* (McGraw–Hill, New York, 2002).
[9]J.-M. Wang, S.-C. Fang, and W.-S. Feng, IEEE J. Solid-State Circuits **29**, 780 (1994).
[10]N. Yokoyama, K. Imamura, S. Muto, S. Hiyamizu, and H. Nishi, Jpn. J. Appl. Phys., Part 2 **24**, L853 (1985).
[11]Y. Takahashi, A. Fujiwara, K. Yamazaki, H. Namatsu, K. Kurihara, and K. Murase, Appl. Phys. Lett. **76**, 637 (2000).
[12]T. Kitade, K. Ohkura, and A. Nakajima, Appl. Phys. Lett. **86**, 123118 (2005).
[13]S.-H. Jhi, S. G. Louie, and M. L. Cohen, Phys. Rev. Lett. **85**, 1710 (2000).
[14]V. Derycke, R. Martel, J. Appenzeller, and Ph. Avouris, Appl. Phys. Lett. **80**, 2773 (2002).
[15]Ph. Avouris, Acc. Chem. Res. **35**, 1026 (2002).
[16]M. Nishisaka, Y. Ochiai, and T. Asano, 56th Annual Device Research Conference Digest (1998), pp. 74–75.
[17]P. J. Herrero, S. Sapmaz, C. Dekker, L. P. Kouwenhoven, and H. S. J. van der Zant, Nature (London) **429**, 389 (2004).
[18]S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, and Ph. Avouris, J. Vac. Sci. Technol. B **20**, 2798 (2002).